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EXAMINER	
LI, AIMEE J	

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2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/716,378	MINE, KAZUMASA	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 and new claims 19-23 have been considered. Claims 1, 3-6, 8-11, 13-15, and 17-18 have been amended as per Applicant's request. New claims 19-23 have been added per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claim 22 is rejected under 35 U.S.C. 102(e) as being taught by Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy). Levy has taught a microprocessor system, comprising:

a. A main processor including an interrupt request reception circuit (Levy Abstract; column 6, line 50 to column 7, line 24; Figure 6; and Figure 7);

b. A co-processor operative under the control of said main processor for autonomously fetching and executing an instruction (Levy Abstract; column 2, lines 35-63; column 8, lines 34-41; column 9, lines 42-46; Figure 2; and Figure 3), said co-processor including an interrupt request generation circuit (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7); and

c. At least one signal line interconnecting said interrupt request generation circuit and said interrupt request reception circuit (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 4-16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy) in view of Schmidt et al., U.S. Patent Number 5,727,227 (herein referred to as Schmidt).

7. Referring to claim 1, Levy has taught a microprocessor system for executing instructions described in a program comprising:

a. A main processor for executing by hardware instructions which belong to a first instruction set (Levy Abstract; column 2, lines 49-63; Figure 2; and Figure 3) and for executing by software instructions which belong to a second instruction set

(Levy Abstract; column 9, lines 46-59; column 10, lines 4-36; Figure 2; and Figure 3); and

b. Said main processor including an interrupt request reception circuit (Levy Abstract; column 6, line 50 to column 7, line 24; Figure 6; and Figure 7);

c. A co-processor operative under the control of said main processor for autonomously fetching an instruction belonging to said second instruction set to execute same by its hardware (Levy Abstract; column 2, lines 35-63; column 8, lines 34-41; column 9, lines 42-46; Figure 2; and Figure 3);

d. Said co-processor including an interrupt request generation circuit, said interrupts request generation circuit being connected to said interrupt request reception circuit by at least one signal line and allowing an interrupt address to be identified in said main processor (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7).

8. Levy has not taught an interrupt vector. Schmidt has taught interrupt vectors (Schmidt column 3, lines 4-42). A person of ordinary skill in the art at the time the invention was made would have recognized that an interrupt vector identifies information, including the address of the interrupt service routine, needed in order to execute the interrupt service routine. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the interrupt vector of Schmidt in the device of Levy to provide the information needed to access the interrupt service routine.

9. Referring to claim 2, Levy has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set which said co-

processor cannot process by itself and issues a notification of said encounter to said main processor to thereby request the main processor to execute said specific instruction (Levy Abstract; column 9, lines 46-59; column 10 ,lines 4-36; Figure 2; Figure 3; Figure 6; and Figure 7).

10. Referring to claims 4-7 and 11, Levy has taught:

    a. Wherein said co-processor issues said notification by dedicated interrupt assigned in advance respectively to a predetermined number of the instructions belonging to said second instruction set which have a higher frequency of execution than the other instructions (Applicant's claims 4) (Levy Abstract; column 6, line 50 to column 7, line 24; Figure 6; and Figure 7)

    b. Wherein said interrupt request reception circuit in said main processor encodes said dedicated interrupts sent from said co-processor (Applicant's claim 11) (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7).

11. Levy has not taught:

    a. Interrupt vectors (Applicant's claim 4)

    b. Wherein at least one of said dedicated interrupt vectors is assigned to a plurality of instructions belonging to said second instruction set (Applicant's claim 5)

    c. Wherein priorities are set to a plurality of said dedicated interrupt vectors (Applicant's claim 6)

    d. Wherein a single instruction is assigned to a given one of said dedicated interrupt vectors to which a higher priority is set, while a plurality of instructions are

assigned to a given one of said dedicated interrupt vectors to which a lower priority is set (Applicant's claim 7)

e. Specify an interrupt handler which corresponds to said specific instruction to be processed (Applicant's claim 11).

12. Schmidt has taught:

a. Interrupt vectors (Applicant's claim 4) (Schmidt column 3, lines 4-42)

b. Wherein at least one of said dedicated interrupt vectors is assigned to a plurality of instructions belonging to said second instruction set (Applicant's claim 5) (Schmidt column 3, lines 4-42).

c. Wherein priorities are set to a plurality of said dedicated interrupt vectors (Applicant's claim 6) (Schmidt column 3, lines 4-42). In regards to Schmidt, the priority is inherent since the current process in the host is interrupted in order for the exception to be completed before the host processor completes the operation it was operating before the interrupt.

d. Wherein a single instruction is assigned to a given one of said dedicated interrupt vectors to which a higher priority is set, while a plurality of instructions are assigned to a given one of said dedicated interrupt vectors to which a lower priority is set (Applicant's claim 7) (Schmidt column 3, lines 4-42). In regards to Schmidt, the table includes information on the interrupts which includes whether the handler routine is one instruction or a plurality of instructions.

e. Specify an interrupt handler which corresponds to said specific instruction to be processed (Applicant's claim 11) (Schmidt column 3, lines 4-42).

13. A person of ordinary skill in the art at the time the invention was made would have recognized that an interrupt vector identifies information, including the address of the interrupt service routine, needed in order to execute the interrupt service routine. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the interrupt vector of Schmidt in the device of Levy to provide the information needed to access the interrupt service routine.

14. Referring to claims 8-10, Levy has taught wherein said co-processor further comprises:

a. A stack memory for holding data generated in the course of execution of an instruction which belongs to said second instruction set (Applicant's claim 8) (Levy Abstract; column 7, lines 61-64; column 11, lines 1-14; and Figure 3);

b. A stack pointer for holding an address of the most recent data in said stack memory (Applicant's claim 8) (Levy column 5, lines 18-42; column 7, lines 29-42; Figure 3; and Figures 8-12);

c. A hardware resource for carrying out a process for updating said stack pointer among processes which take place in the course of execution of said specific instruction (Applicant's claim 8) (Levy column 12, lines 26-31 and Figures 8-12);

d. A program counter for holding an address of an instruction which is currently processed and belongs to said second instruction set (Applicant's claim 9) (Levy column 5, lines 18-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7);

e. A hardware resource for carrying out a process for updating said program counter among processes which take place in the course of execution of said specific instruction (Applicant's claim 9) (Levy column 5, lines 18-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7); and

f. A status register for holding information indicative of a need of said notification and wherein said main processor periodically accesses said status register to recognize, from content of said status register, that said co-processor has encountered said specific instruction to thereby execute said specific instruction (Applicant's claim 10) (Levy column 5, lines 18-42; column 7, lines 29-64; column 8, lines 21-24; Figure 3; Figure 6; and Figure 7).

15. Referring to claims 12-16, Levy has taught

a. An instruction queue for holding a fetched instruction which belongs to said second instruction set (Applicant's claim 12) (Levy column 8, lines 34-41; column 9, lines 42-59; and Figure 3);

b. Wherein said main processor refers to said instruction queue of said co-processor to specify an interrupt handler which corresponds to said specific instruction to be executed (Applicant's claim 12) (Levy column 9, lines 42-59; Figure 6; and Figure 7);

c. Wherein said co-processor includes a stack architecture (Applicant's claim 13) (Levy Abstract; column 5, lines 31-59; and Figure 3);

d. A stack memory provided outside said co-processor (Applicant's claim 14) (Levy Abstract; column 7, lines 61-64; column 11, lines 1-14; and Figure 3),

e. A stack-top register for holding a predetermined number of top data of stack data (Applicant's claim 14) (Levy column 5, lines 18-42; column 7, lines 29-42; Figure 3; and Figures 8-12);

f. A cache memory provided between said stack memory and said stacktop register for caching a part of data held in said stack memory (Applicant's claim 15) (Levy column 11, lines 1-14; Figure 3; and Figure 10); and

g. Wherein said co-processor detects a predetermined instruction for which stack data needs to be manipulated over said stack-top register and said stack memory (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-12),

h. Whereupon said co-processor moves contents of said stack-top register to said stack memory (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-12) and thereafter requests said main processor to execute said predetermined instruction (Applicant's claim 16) (Levy column 6, lines 50 to column 7, line 24), said main processor referring to contents of said stack memory, to which said contents of said stack-top register have been moved (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-12), to thereby execute said predetermined instruction (Applicant's claim 16) (Levy column 12, lines 1-43 and Figures 8-12).

In regards to Levy, the example embodiment completes stack instructions in the co-processor, but, as is stated in column 6, line 50 to column 7, line 24 of Levy, the co-processor may send these instructions to the host.

16. Referring to claim 18, Levy has taught a program memory in which instructions belonging to said second instruction set are contained, wherein said co-processor further comprises:

a. A program counter for holding an address of an instruction that is currently processed and belongs to said second instruction set (Levy column 5, lines 8-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7);

b. An instruction queue for holding instructions which belong to said second instruction set (Levy column 8, lines 34-41; column 9, lines 42-59; and Figure 3); and

c. An instruction fetch circuit for fetching an instruction belonging to said second instruction set from said program memory using a value contained in said program counter as its address and for setting the fetched instruction to said instruction queue (Levy column 5, lines 8-42; column 7, lines 29-42; column 8, liens 34-41; column 9, lines 42-59; Figure 3; Figure 6; and Figure 7).

17. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy) in view of Schmidt et al., U.S. Patent Number 5,727,227 (herein referred to as Schmidt), as applied to claim 2 above, and in further view of Irwin, U.S. Patent Number 4,695,945 (herein referred to as Irwin). Levy has not explicitly taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set for which data presently under the control of said main processor needs to be handled to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself. However, Levy has taught wherein said

co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself (Levy Abstract; column 9, lines 46-59; column 10, lines 4-36; Figure 2; Figure 3; Figure 6; and Figure 7). Irwin has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set for which data presently under the control of said main processor needs to be handled to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself (Irwin Abstract; column 2, lines 39-64). A person of ordinary skill in the art at the time the invention was made, and as stated in Irwin, would have recognized that detecting this type of encounter is necessary to identify possible problems of contention for system resources (Irwin column 2, lines 22-24). By identifying these encounters, the processors resolve the resource contention and allow for processing to continue. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the encounter detection of Irwin in the device of Levy to resolve resource contention.

18. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy) in view of Schmidt et al., U.S. Patent Number 5,727,227 (herein referred to as Schmidt), as applied to claim 1 above, and in further view of Yamanaka, U.S. Patent Number 4,774,625 (herein referred to as Yamanaka). Levy has not taught a plurality of coprocessors in correspondence with a plurality of processes described in a program. Yamanaka has taught a plurality of coprocessors in correspondence with a plurality of processes described in a program (Yamanaka column 1, line 21 to column 2, line 28; Figure 1; and Figure 2). A person of ordinary skill in the art at the time the invention was made would

have recognized that the plurality of coprocessors would allow for more operations to be executed simultaneously, thereby increasing speed of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the plurality of coprocessors of Yamanaka in the device of Levy to increase processor speed.

19. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy) in view of Irwin, U.S. Patent Number 4,695,945 (herein referred to as Irwin).

20. Referring to claim 19, Levy has taught a method of processing computer programs, said method comprising:

a. Using a main processor for executing hardware instructions which belong to a first instruction set (Levy Abstract; column 2, lines 49-63; Figure 2; and Figure 3) and for executing software instructions which belong to a second instruction set (Levy Abstract; column 9, lines 46-59; column 10, lines 4-36; Figure 2; and Figure 3);

b. Using a co-processor, operative under the control of said main processor, for autonomously fetching instructions belonging to said second instruction set to execute the fetched instructions by its hardware (Levy Abstract; column 2, lines 35-63; column 8, lines 34-41; column 9, lines 42-46; Figure 2; and Figure 3); and

c. Generating an interrupt request from said co-processor to said main processor (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7) when said co-processor detects encountering one of the

instructions belonging to said second instruction set which said co-processor cannot process by itself, thereby requesting that said main processor execute said instruction (Levy Abstract; column 9, lines 46-59; column 10 ,lines 4-36; Figure 2; Figure 3; Figure 6; and Figure 7),

d. Wherein said interrupt request comprises a signal on at least one signal line between said main processor and said co-processor (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7).

21. Levy has not explicitly taught wherein said co-processor is unable to execute at least one instruction in said second instruction set. However, Levy has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself (Levy Abstract; column 9, lines 46-59; column 10, lines 4-36; Figure 2; Figure 3; Figure 6; and Figure 7). Irwin has taught wherein said co-processor is unable to execute at least one instruction in said second instruction set (Irwin Abstract; column 2, lines 39-64). A person of ordinary skill in the art at the time the invention was made, and as stated in Irwin, would have recognized that detecting this type of encounter is necessary to identify possible problems of contention for system resources (Irwin column 2, lines 22-24). By identifying these encounters, the processors resolve the resource contention and allow for processing to continue. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the encounter detection of Irwin in the device of Levy to resolve resource contention.

22. Referring to claim 20, Levy has taught converting said encoded signal. into an interrupt handler address in said main processor (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7). In regards to Levy, it is inherent that the main processor would convert the encoded signal into an interrupt handler, since the main processor must be able to determine which instruction is being executed and the address of the correct handler in order to correctly execute the instruction which cannot be executed by the co-processor, as is stated in Levy column 9, lines 46-59.

23. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy) in view of Irwin, U.S. Patent Number 4,695,945 (herein referred to as Irwin), as applied to claim 20 above, and in further view of Schmidt et al., U.S. Patent Number 5,727,227 (herein referred to as Schmidt). Levy has not taught wherein said at least one signal line comprises a plurality of signal lines. Schmidt has taught wherein said at least one signal line comprises a plurality of signal lines (Schmidt column 3, lines 4-42). In regards to Schmidt, it is inherent there would be a plurality of signal lines since a vector is more than one bit of data, which requires more than one signal line since a signal line represents one bit. A person of ordinary skill in the art at the time the invention was made would have recognized that an interrupt vector represented by a plurality of signal lines identifies information, including the address of the interrupt service routine, needed in order to execute the interrupt service routine. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the interrupt vector of Schmidt in the device of Levy to provide the information needed to access the interrupt service routine.

24. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy), as applied to claim 22 above, and in further view of Schmidt et al., U.S. Patent Number 5,727,227 (herein referred to as Schmidt). Levy has not taught wherein said at least one signal line comprises a plurality of signal lines. Schmidt has taught wherein said at least one signal line comprises a plurality of signal lines (Schmidt column 3, lines 4-42). In regards to Schmidt, it is inherent there would be a plurality of signal lines since a vector is more than one bit of data, which requires more than one signal line since a signal line represents one bit. A person of ordinary skill in the art at the time the invention was made would have recognized that an interrupt vector represented by a plurality of signal lines identifies information, including the address of the interrupt service routine, needed in order to execute the interrupt service routine. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the interrupt vector of Schmidt in the device of Levy to provide the information needed to access the interrupt service routine.

Response to Arguments

25. Applicant's arguments with respect to claims 19-23 have been considered but are moot in view of the new ground(s) of rejection. In regards to claims 1-18, Applicant's arguments filed 24 March 2004 have been fully considered but they are not persuasive.

26. Applicant argues in essence on page 12 "Schmidt requires an interrupt co-processor to handle the interrupt vector. There is no such interrupt co-processor in Levy." This has not been found persuasive. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what

the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this particular instance, it is the concept of interrupt vectors and how they are used suggested by Schmidt which has been relied upon and taken from Schmidt. The *entire* invention of Schmidt would not necessarily be incorporated into Levy, but only the portion teaching the above.

27. Applicant argues in essence on page 12 "Second, and even more important, the technique used in Schmidt would change the principle of operation in Levy." This has not been found persuasive. This assertion was made without explanation or evidence by Applicant and/or Applicant's representative. Applicant and/or Applicant's representative has not provided evidence and/or explanation for this assertion, and the Examiner cannot determine why this assertion was made. The co-processor in Levy would still interrupt the main processor and the main processor would still execute the interrupt in some manner that was not specified. When combined with Schmidt, the interrupts manner of execution would now use interrupt vectors and the methods related to interrupt vectors.

28. Applicant argues in essence on page 13 "The correct standard of use is: whether the prior art reference suggests the combination. The standard used by the Examiner is clearly a statement of improper hindsight." In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21

USPQ2d 1941 (Fed. Cir. 1992). In this case, the knowledge is generally available to one of ordinary skill in the art. The test of obviousness is:

> "whether the teachings of the prior art, taken as a whole, would have made obvious the claimed invention," In re Gorman, 933 F.2d at 986, 18 USPQ2d at 1888.
>
> Subject matter is unpatentable under section 103 if it "'would have been obvious . . . to a person having ordinary skill in the art.' While there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that the cited references or prior art specifically suggest making the combination." In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988).
>
> "Such suggestion or motivation to combine prior art teachings can derive solely from the existence of a teaching, which one of ordinary skill in the art would be presumed to know, and the use of that teaching to solve the same [or] similar problem which it addresses." In re Wood, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979).
>
> "In sum, it is off the mark for litigants to argue, as many do, that an invention cannot be held to have been obvious unless a suggestion to combine prior art teachings is found in a specific reference."

29. Entire quote from In re Oetiker, 24 USPQ2d 1443 (CAFC 1992). In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense

necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

30. Applicant' argues in essence on page 13

> "Relative to the urged combination of Yamanaka with Levy, such combination would be improper since the Yamanaka operation processors, 17a, 17b, 17c are slave processing units, rather than the autonomous co-processors of Levy".

31. This has not been found persuasive. Again, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, it is the suggestion that a device may have a plurality of processors each designated to a specific operation in the program. Yamanaka has taught co-processors

which execute certain types of operations under the control of the main processor. A slave processor is not necessarily non-autonomous, because a slave processor independently executes an instruction by using its own hardware and does not rely upon the main processor's hardware to execute the instruction.

Conclusion

32. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

33. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
June 10, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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